Remarks

Claims 39-41, 57-59, and 71-74 are pending.

Claims 39 and 58 are independent claims. Claims 40, 41, 71, and 72 depend from independent claim 39 and claims 58, 59, 73, and 74 depend from independent claim 57.

The Examiner has indicated that claims 41 and 59 would be allowable if rewritten in independent form.

The Examiner has rejected claims 39, 40, 57, and 58 under 35 U.S.C. § 102(e) over the first embodiment of Kimura (U.S. 2002/0192901).

Each of independent claims 39 and 57 requires the ferroelectric device level to completely encompass at least one ferroelectric capacitor structure comprising a top electrode having an electrical contact area, a bottom electrode and ferroelectric dielectric material disposed between the top and bottom electrodes. The claimed ferroelectric device level further encompasses a ferroelectric isolation layer structure that is disposed over at least a portion of the top electrode of the at least one ferroelectric capacitor structure and that electrically isolates non-electrical contact areas of the at least one ferroelectric capacitor structure from overlying and adjacent electrical structures. The Examiner has asserted that Kimura's memory device includes a "ferroelectric device level 14 including at least one ferroelectric capacitor 19-20, and an overlying ferroelectric isolation layer 16."

Element 14 in Kimura's memory device, however, is a dielectric layer that is aligned only with the lower portions of the two ferroelectric capacitors shown in FIG. 1 of Kimura. No one of ordinary skill in the art at the time of the invention would have considered the dielectric layer 14 to be a "ferroelectric device level 14 that completely encompasses at least one ferroelectric capacitor structure comprising a top electrode having an electrical contact area, a bottom electrode and ferroelectric dielectric material disposed between the top and bottom electrodes," as now recited in independent claims 39 and 57. Indeed, Kimura clearly shows in FIG. 1 that the ferroelectric capacitor structures extend above the dielectric layer 14 and therefore, in no sense of the term, could these ferroelectric capacitor structures be considered to be "completely encompassed" by the dielectric layer 14.

In addition, the Examiner has asserted that layer 16 corresponds to the claimed ferroelectric isolation structure. However, layer 16 is not disposed over at least a portion of the top electrode of the at least one ferroelectric capacitor structure. Instead, layer 16 lies under the top portion of plate electrode 21 and adjacent to the top portions of capacitor

dielectrics 20 and lower electrodes 19. In addition to not being disposed over at least a portion of the top electrode of at least one ferroelectric capacitor structure, layer 16 does not electrically isolate non-electrical contact areas of the at least one ferroelectric capacitor structure from overlying electrical structures, as now recited in independent claim 39 and 57.

Dielectric layer 22 is the only layer in Kimura's memory device that overlies at least a portion of a top electrode of at least one ferroelectric capacitor. Accordingly, in order to find in Kimura's memory device a "ferroelectric device level" consistent with claims 39 and 57, one must label the structure formed from the lower electrode 19, the capacitor dielectric 20 and the plate electrode 21 as the claimed "ferroelectric capacitor structure", and the dielectric layer 22 as the claimed "overlying ferroelectric isolation structure". In this case, however, as shown in FIGS. 1 and 16, there is only one metallization level 24 (corresponding to the claimed "first metal level") disposed over the ferroelectric device level (consisting of elements 14, 15, 16, 17, 18, 19, 20, 21, 22, and 23). Therefore, Kimura's memory device does not include an inter-level dielectric level disposed over the first wiring level, nor does it include a second wiring level disposed over the inter-level dielectric level, as recited in each of independent claims 39 and 57.

For at least these reasons, the Examiner's rejection of independent claims 39 and 57 under 35 U.S.C. § 102(e) over Kimura now should be withdrawn.

Claims 40, 71, and 72 incorporate the features of independent claim 39 and claims 58, 73, and 74 incorporate the features of independent claim 57. Therefore, claims 40, 71, 72, 58, 73, and 74 are patentable for at least the same reasons explained above. Claims 71-74 also are patentable for the following additional reasons.

Each of claims 71 and 73 recites that between the ferroelectric device level and the transistor isolation layer is free of any interposing wiring level. As shown in FIG. 1, the first embodiment of Kimura includes a first wiring level (consisting of layers 9 and 10) and a second wiring level (consisting of layers 11 and 12), both of which are interposed between a ferroelectric device level (consisting of layers 19, 20, 21, 22) a transistor isolation layer 8. For at least this additional reason, claims 71 and 73 are patentable over Kimura.

Each of claims 72 and 74 recites that throughout the ferroelectric isolation structure the at least one via extending therethrough is laterally sized larger than the corresponding contact via of the transistor isolation structure. Kimura does not teach or suggest such a feature. For at least this additional reason, claims 72 and 74 are patentable over Kimura.

For the reasons explained above, all of the pending claims are now in condition for allowance and should be allowed.

Charge any excess fees or apply any credits to Deposit Account No. 50-1078.

Respectfully submitted,

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